What is claimed is:

1. A semiconductor package comprising:

a metal plate; and

a wiring substrate including an insulating substrate, signal wiring layers formed on a one surface of the insulating substrate, and a ground plane formed integrally on another surface of the insulating substrate, the wiring substrate whose surface of the ground plane side is adhered onto the metal plate;

wherein the signal wiring layer is constructed by a wiring line portion and a connection pad portion whose width is thicker than a width of the wiring line portion, and a non-forming portion is provided in a portion of the ground plane, which corresponds to the connection pad portion.

2. A semiconductor package according to claim 1, wherein the non-forming portion of the ground plane is formed as a hollow, or is filled with a resin layer.

3. A semiconductor package according to claim 1, wherein the non-forming portion of the ground plane is formed as a hollow, and a resin layer is interposed between the non-forming portion and the metal plate.

4. A semiconductor package according to claim 3, wherein the resin layer is adjusted to have a thickness that attains an impedance matching between the wiring line portion and the connection pad portion.

5. A semiconductor package according to claim 1,

wherein a recess portion is further provided in a portion of the metal plate, which corresponds to the non-forming portion of the ground plane,

6. A semiconductor package according to claim 1, further comprising:

a ground wiring layer formed on the one surface of the insulating substrate adjacently to the signal wiring layer; and

wherein the ground wiring layer, the ground plane, and the metal plate are electrically connected mutually to constitute an integral equal-potential ground.

7. A semiconductor package according to claim 6, wherein the ground wiring layer and the ground plane and the metal plate are connected electrically via a through hole in which a conductor is filled.

8. A semiconductor package according to claim 6, wherein the ground wiring layer and the ground plane and the metal plate are connected electrically by a conductor that is provided in an area that reaches the metal plate from a side wall of an end portion of the wiring substrate, in which side surfaces of the ground wiring layer and the ground plane are exposed.

9. A semiconductor package according to claim 5, wherein the non-forming portion of the ground plane and the recess portion of the metal plate are formed as a hollow, or are filled with a resin layer.

10. A semiconductor package comprising:

a metal plate; and

a wiring substrate including an insulating substrate, and a signal wiring layer formed on a one surface of the insulating substrate, the wiring substrate whose another surface is adhered onto the metal plate;

wherein the signal wiring layer is constructed by a wiring line portion and a connection pad portion whose width is thicker than a width of the wiring line portion, and a recess portion is provided in a portion of the metal plate, which corresponds to the connection pad portions.

11. A semiconductor package according to claim 10, further comprising:

a ground wiring layer formed on the one surface of the insulating substrate adjacently to the signal wiring layer; and

wherein the ground wiring layer and the metal plate are electrically connected mutually to constitute an integral equal-potential ground.

12. A semiconductor package according to claim 10, wherein the recess portion of the metal plate is formed as a hollow, or is filled with a resin layer.

13. A semiconductor package according to claim 5, wherein the recess portion of the metal plate is formed to have a cylindrical, hemispherical, or cone-type shape.

14. A semiconductor package according to claim 5, wherein the recess portion of the metal plate is adjusted

to have a depth that attains an impedance matching between the wiring line portion and the connection pad portion.

15. A semiconductor package comprising:

a metal plate; and

a wiring substrate including a film substrate, and a signal wiring layer formed on a one surface of the film substrate and the signal wiring layer having a connection pad portion which is jointed to a bump, the film substrate whose another surface is adhered onto the metal plate;

wherein stress applied to the bump is relaxed by providing a recess portion in a portion of the metal plate, which corresponds to the connection pad portion.

16. A semiconductor package according to claim 15, further comprising:

a ground plane formed integrally on another surface of the film substrate; and

wherein a non-forming portion is provided in a portion of the ground plane, which corresponds to the connection pad portion.

17. A semiconductor package according to claim 15, wherein the recess portion of the metal plate is formed as a hollow, or is filled with an elastic body or phenol resin.

18. A semiconductor package according to claim 1, wherein the metal plate has a chip mounting portion on

which a semiconductor chip is mounted in a predetermined center portion, and the wiring substrate is adhered to a peripheral portion of the metal plate except the chip mounting portion.

19. A semiconductor device comprising:

the semiconductor package set forth in claim 18; and

a semiconductor chip having a connection electrode on a surface side, wherein a back surface side of the semiconductor chip is adhered onto the chip mounting portion, and the connection electrode is connected electrically to a wiring layer of the one surface of the wiring substrate.

20. A semiconductor device according to claim 19, wherein a cavity is provided in the chip mounting portion of the metal plate of the semiconductor package, and the semiconductor chip is adhered onto a bottom portion of the cavity.

21. A semiconductor device according to claim 19, further comprising:

a bump jointed to the connection pad portion of the one surface of the wiring substrate.